Preliminary Specification

P1727/66

Low Power Notebook LCD Panel EMI Reduction IC

FEATURES

- FCC approved method of EMI attenuation
- Generates a low EMI spread spectrum of the input clock frequency
- Optimized for frequency range:
  P1727X: 20MHz to 40MHz
  P1766X: 40MHz to 80MHz
- Internal loop filter minimizes external components and board space
- 8 different frequency deviations ranging from **+/-0.625% to –3.50%**
- Low inherent cycle-to-cycle jitter
- 3.3V operating voltage
- CMOS/TTL compatible inputs and outputs
- ***Ultra low power*** CMOS design
  TBD mA @3.3V, 54 MHz
  TBD mA @3.3V, 65 MHz
- Supports notebook VGA and other LCD timing controller applications
- Available in 8 pin SOIC and TSSOP
- Qualified for Industrial Temp Spec. (+85C)

PRODUCT DESCRIPTION

The P1727/66 is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The P1727/66 reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream (clock and data dependent signals). The P1727/66 allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P1727/66 modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal’s bandwidth is called “spread spectrum clock generation”.

The P1727/66 uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all-digital method.

APPLICATIONS

The P1727/66 is targeted towards notebook LCD displays, other displays using an LVDS interface, PC peripheral devices, and embedded systems.

Figure 1 – P1727/66 Pin Diagram

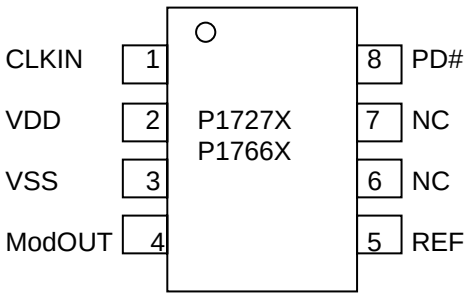

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Figure 2 – P1727/66 Block Diagram

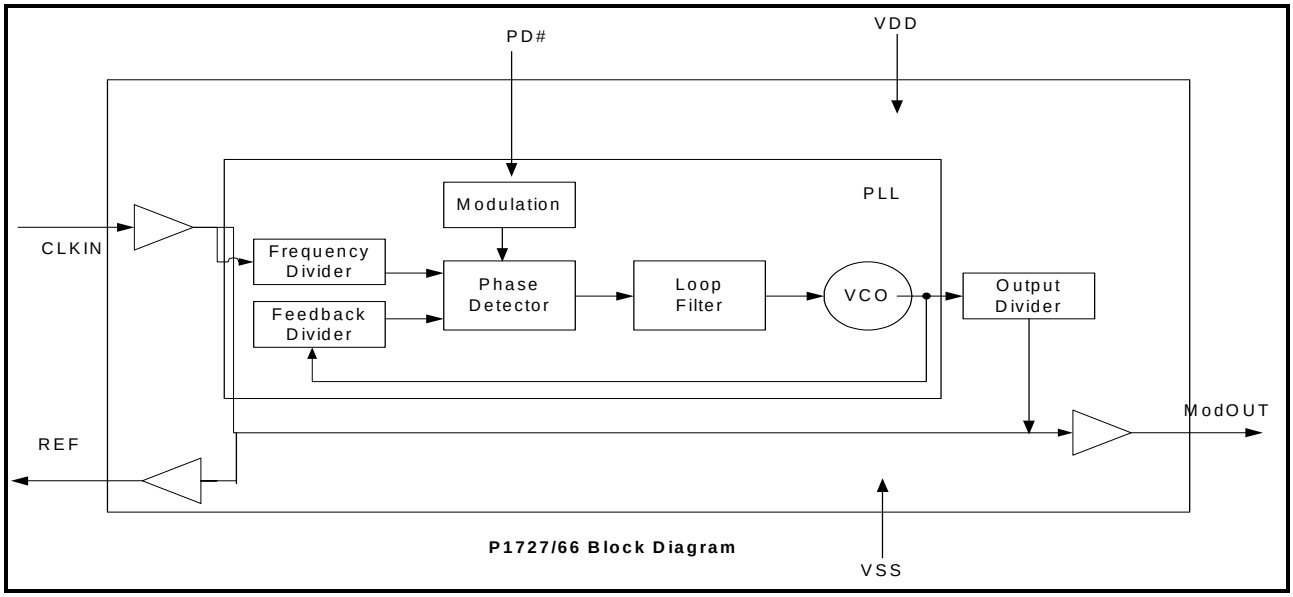


Table 1-Power Down Selection

PD#	Spread Spectrum	ModOut	PLL	Mode
0	N/A	Disabled	Disabled	Power Down
1	ON	Normal	Normal	Normal

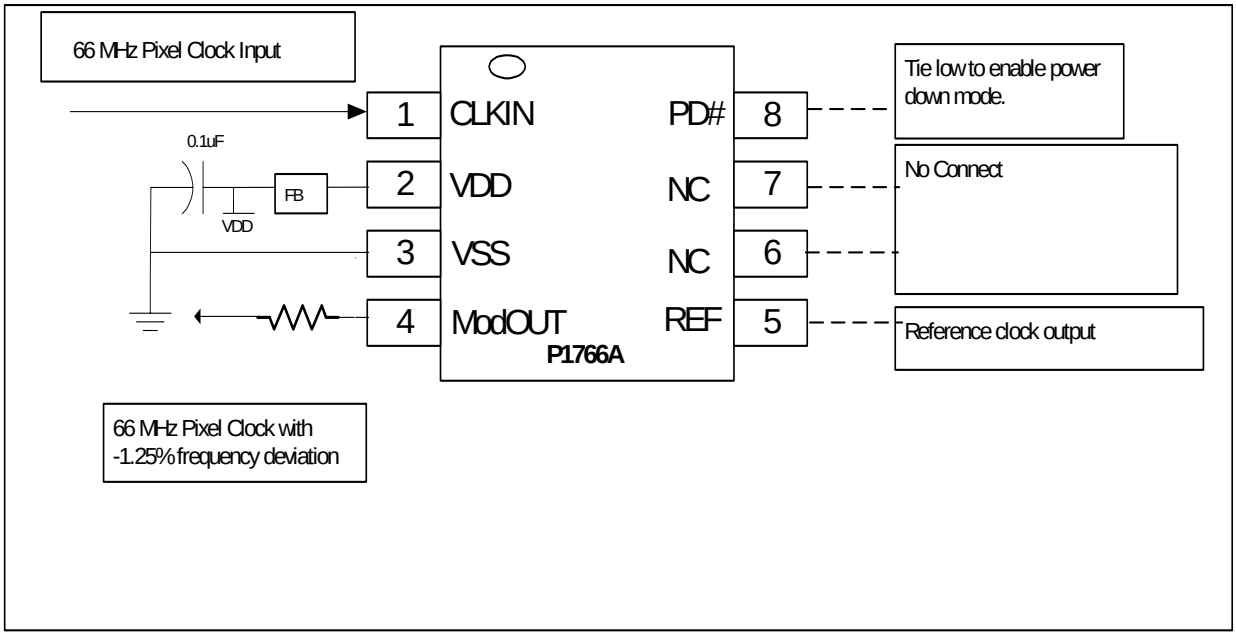
Table 2 Frequency Deviation Selection

P/N	Deviation	P/N	Deviation
P1727/66A	**-1.25%**	**P1727/66E**	**+/-0.625%**
P1727/66B	**-1,75%**	**P1727/66F**	**+/-0.875%**
P1727/66C	**-2.50%**	**P1727/66G**	**+/-1.25%**
P1727/66D	**-3.50%**	**P1727/66H**	**+/-1.75%**

PIN DESCRIPTION

PIN #	Name	Type	Description
1	CLKIN	I	Connect to externally generated clock signal.
2	VDD	P	Connect to +3.3V
3	VSS	P	Ground Connection. Connect to system ground.
4	ModOut	O	Spread Spectrum Clock Output.
5	REF	I	Reference output.
6	N/C	N/C	No connect
7	N/C	N/C	No connect
8	PD#	I	Pull low to enable Power Down Mode. This pin has an internal pull-up resistor.

Figure 3 – P1727/66 Schematic for notebook VGA application



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +125	ºC
T_A	Operating Temperature	0 to +70	ºC

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GND – 0.3	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	V_{DD} + 0.3	V
I_{IL}	Input Low Current (100 KΩ input pull-up resistor on inputs SR0, 1)	-	-	-35	µA
I_{IH}	Input High Current (100 KΩ input pull-down resistor on input SSON)	-	-	35	µA
I_{XOL}	XOUT Output Low Current (@ 0.4V, V_{DD} = 3.3V)	-	3	-	mA
I_{XOH}	XOUT Output High Current (@ 2.5V, V_{DD} = 3.3V)	-	3	-	mA
V_{OL}	Output Low Voltage (V_{DD}=3.3V, I_{OL} = 20 mA)	-	-	0.4	V
V_{OH}	Output High Voltage (V_{DD}=3.3V, I_{OH} = 20 mA)	2.5	-	-	V
I_{DD}	Static Supply Current Standby Mode	-	TBD	-	mA
I_{CC}	Dynamic Supply Current Normal Mode (3.3V and 10 pF loading)	TBD f_{IN-min}	TBD f_{IN-typ}	TBD f_{IN-max}	mA
V_{DD}	Operating Voltage	TBD	3.3	TBD	V
t_{ON}	Power Up Time (First locked clock cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock Output Impedance	-	50	-	Ω

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency: P1727-X P1766-X	20 40	-	40 80	MHz
t_{LH} Note 1	Output Rise Time (measured at 0.8V to 2.0V)	0.7	0.9	1.1	ns
t_{HL} Note 1	Output Fall Time (measured at 2.0V to 0.8V)	0.6	0.8	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	TBD	ps
t_D	Output Duty Cycle	45	50	55	%

Note1: t_{LH} and t_{HL} are measured into a capacitive load of 15pF

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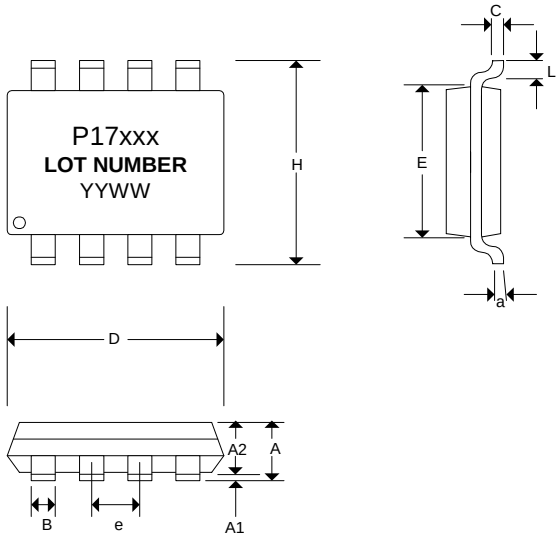
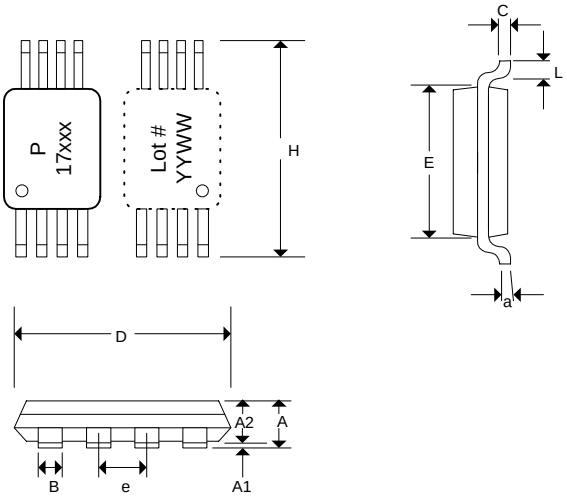
Figure 6 – Mechanical Package Outline, (8 Pin SOIC)



	INCHES			MILLIMETERS		
SYMBOL	**MIN**	**NOR**	**MAX**	**MIN**	**NOR**	**MAX**
A	0.057	0.064	0.071	1.45	1.63	1.80
A1	0.004	0.007	0.010	0.10	0.18	0.25
A2	0.053	0.061	0.069	1.35	1.55	1.75
B	0.012	0.016	0.020	0.51	0.41	0.31
C	0.004	0.006	0.001	0.10	0.15	0.25
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.164	3.75	3.95	4.15
e	0.050 BSC			1.27 BSC		
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.012	0.020	0.028	0.30	0.50	0.70
a	0°	5°	8°	0°	5°	8°

Figure 7 – Mechanical Package Outline, (8 Pin TSSOP)



	INCHES			MILLIMETERS		
SYMBOL	**MIN**	**NOR**	**MAX**	**MIN**	**NOR**	**MAX**
A	-	-	0.047	-	-	1.10
A1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	-	8°	0°	-	8°

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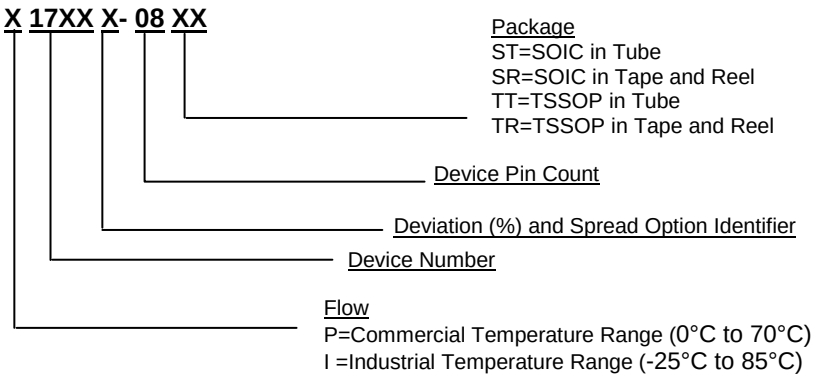
Ordering Information:



Example:

ORDERING INFORMATION

Ordering Number	Marking	Package Type	Qty. / Reel	Temperature
P1727/66X-08ST	P1727/66X	8 PIN SOIC, TUBE		0°C TO 70°C
P1727/66X-08SR	P1727/66X	8 PIN SOIC, TAPE & REEL	2,500	0°C TO 70°C
P1727/66X-08TT	P1727/66X	8 PIN TSSOP, TUBE		0°C TO 70°C
P1727/66X-08TR	P1727/66X	8 PIN TSSOP, TAPE & REEL	2,500	0°C TO 70°C